APPENDIX

SIGNAL AND POWER PIN DESCRIPTION

Pin Name (I/O Type)	*Pin Description*
RXL_CLK622P/N	Receive Line Clock 722MJz (Positive and Negative). 622MHZ input clock driven from the line side OC-192 demux chip. This clock is used to derive all timing for the receive signal path. This clock is divided by four internally to create the RXD (3:0)_CLK155P/N AND RXD_REFCK155P/N 144 MHz output clocks. This clock is the reference for the RXL_DATP/N [15:0] input data bus.
RXL_DATP/N [15:0] (Input)	Receive Line Data (Positive and Negative). Parallel 16-bit line side data input from external OC-192 demux chip. Data is 622MHz synchronous with respect to RXL-CLK622P/N. Input data is NOT BYTE ALIGNED. This inputs are latched on the rising edge of RXL-CLK622P. RXL_DATP/N[15] is the MSB (first bit received).
TXL_CLK622P/N (Output)	Transmit Line Input Clock 622MHz (Positive and Negative). 622MHz input clock driven from the line side OC-192 mux chip (or from a system clock generation circuit). This clock is used to drive all timing for the transmit path. This clock is divided by four internally to generate the TXD{3:0}_CLK155P/N 155MHz output clocks. This clock is the reference for the TXL_DATP/N [15:0] output data bus. This signal or the 155MHz version below will be used as the input to the PLL.
TXL_DCLK622P/N (Output)	Transmit Line Data Clock 622MHz (Positive and Negative). 622MHz output clock that is centered in the TXL_DATP/N [15:0] data bus eye. This clock is fed into a PLL externally and is used as an input to the OC-192 mux device as a reference for the TXL-DATP/N[15:0] output data bus. This signal may be used in lieu of the TXL_DCLK622P/N clock as the input to the external de-jitter PLL.
TXL_DATP/N[15:0] (Output)	Transmit Line Output DATa (Positive and Negative). Parallel 16-bit line side data output to external OC-192 mux chip. Data is 622MHZ synchronous with respect to TXL_DCLK622P. TXL_DATP/N[15] is the most significant bit corresponding to the first bit transmitted.
RXD{3:0}_CLK155P/N	Receive Demux {Ports 3:0} Output ClocK 155MHz (Positive and Negative). 155MHz output clocks normally derived from the RXL_CLK622P/N input. This clock is replicated for each of the four demux side output ports of the front-end ASIC chip (i.e., a single point to point clock pin pair is provided for each of the

Pin Name (I/O Type)	*Pin Description*
	downstream OC-48 processors). This clock is the reference for the RXD {3:0}_DAT[15:0] output data bus which is registered on the rising edge of RXD {3:}_CLK155P.
RXD_REFCK155P/N (Output)	Receive Demux Output REFerence Clock 155MHz output clock normally derived from the RXL_CLK622P/N input. This clock is a copy of the RXD {3:0}_CLK155P/N outputs and is provided as a line rate 155MHz reference clock source.
RXD {3:0}_DAT[15:0] (Output)	Receive Demux {Ports 3:0} Output DATa. Parallel 16-bit demux side data output to external OC-48 processor chips. Data is 155MHz synchronous with respect to RXD {3:0}_CLK155P/N. The RXD {3:0)_DAT[15:0] output register changes on the rising edge RXD{3:0}_CLK155P. RXD {3.0}_DAT[15] is the most significant big corresponding to the first bit transmitted. These output buggers may be optionally operated at CMOS levels when the RXD-DMOS control bit in the G-CRO register is set.
RXD(3:0)_BPCLKP/N (Output)	Receive Demux {Ports 3:0} BackPlane ClocK (Positive and Negative). 155MHz output clocks derived from the BP-CLK155P/N input or from a divide by four version of the TXL_CLK622P/N clock input. This clock is replicated four times on the front-end ASIC chip (i.e., a single point to point clock pin pair is provided for each of the downstream OC-48 processors). These pins should be connected to the RO_CLK 155P/N backplane side clock inputs of the downstream OC-48 processors. This clock is the reference for the RXD{3.0}_BPSYNC output sync pins.
RXD{3.0}_BPSYNC (output)	Receive Demux {Ports 3:0}BackPlane SYNC. Sync pins provided to the backplane side port of the OC-48 processors to synchronize all OC-48 processors backplane framing together. (These signals are provided to keep the OC-192 signal sync'd closely enough together such that the signal can be reassembled after having passed through the matrix.) The location of these sync pins in time is controlled by the BP_FRSYNC input pin. These pins should be connected to the RO_FR_SYNC inputs of the downstream OC-48 processors.
BP-CLK155P/N (Input)	BackPlane Input ClocK 155MHz (Positive and Negative). 155MHz input clock used to (optionally) generate the four RXD{3:0}_BPCLKP/N output clocks. This input is used as the reference for the RXD {3:0}_BPCLKP/N outputs when the SEL_BP_CLK control bit in the G_CR- register is set to a '1'.
BP-FRSYNC (Input)	BackPlane Frame SYNC. Signal used to synchronize the backplane ports of the four OC-48 processors. This input is used to generate the four RXD{3:0}_BPSYNC output signals.

Pin Name (I/O Type)	*Pin Description*
FB_FAILB[1.0] <or> *Test (Output)	FoRCe FRAME. Signal used to indicate a front-end ASIC condition that requires the downstream OC-48 processors to reacquire frame. The 1 and 0 pins of this signal are redundant copies such that each pin only drives two of the four downstream OC-48 processors. These pins should be connected to the FRC_FRAME inputs of the OC-48 processors. These pins, when active, are a frame synchronous positive pulse with a pulse width of four 155MHz clocks. These output pins are considered to be received asynchronously at the downstream OC-48 processors to which they connect.
FRC_FRAME [1.0] (Output)	FoRCe FRAME. Signal used to indicate a front-end ASIC condition that requires the downstream OC-48 processors to reacquire frame. The 1 and 0 pins of this signal are redundant copies such that each pin only drives two of the four downstream OC-48 processors. These pins should be connected to the FRC-FRAME inputs of the OC-48 processors. These pins, when active, are a frame synchronous positive pulse with a pulse width of four 155MHz clocks. These output pins are considered to be received asynchronously at the downstream OC-48 processors to which they connect.
TXD{3.0}_CLK155P/N (Output)	Transmit Demux (Ports 3:0) Output ClocK 155MHz (Positive and Negative). 155MHz output clocks (normally) derived from a divide-by-four of the TXL_CLK622P/N input. This clock is replicated for each of the four demux side input ports of the front-end ASIC chip (i.e., a single point to point clock pin pair is provided for each of the upstream OC-48 processors). These clocks provide the 155MHz clock inputs to the OC-48 processors TO ports and should be connected to the TO_CLK155P/N inputs on the OC-48 processors.
TXD{3:0}_DAT[15:0] (Input)	Transmit Demux {Ports 3:0} Input DATa (Positive). Parallel 16-bit demux side data input from external OC-48 processors. Data is 155 MHz synchronous with respect to TXD{3.0}_DCKLINP/N. The TXD{3:0}_DAT[15:0] input data is latched into a phase aligning FIFO using the TXD{3:0}_DCLKINP clock signals. TXD{3.0}_DAT[15] is the most significant bit corresponding to the first it received. These inputs are always 16-bit aligned data (except in the loopback mode).
TXD{3:0}_DCLKINP/N (Input)	Transmit Demux {Ports 3:0} Data ClocK Input (Positive and Negative). 155MHz input clocks delivered from the four TO_CLKOUTP/N pin pairs on the upstream OC-48 processors. This clock is replicated for each of the four TXD input ports of the front-end ASIC chip (i.e., a single point to point clock pin pair is

Pin Name (I/O Type)	*Pin Description*
	provided for each of the upstream OC-48 processors). These clocks are the reference for the TXD{3:0}_DAT[15:0] input data buses, which are latched on the rising edge of TXD {3:0}_DCLKINP. These pins are used to support the contra-clocking interface of the front-end ASIC device.
TXD{3:0}_FRLOC (Input)	Transmit Demux {Ports 3:0} Frame LOCation. Signal used by the front-end ASIC to determine frame location of the received data on the TXD ports. (Inclusion of this signal eliminates the need for a framer on the TXD input data ports.) These signals are driver synchronously with the TXD {3:0}_DCLKINP/N signals. These signals are asserted for a single 155MHz clock period when active.
TXD{3:0}_FRSYNC (Output)	Transmit Demux {Ports 3:0} Frame SYNC. Signal used to reset the downstream OC-48 processors input framers and to force them to reacquire framing. This signal is used to force all downstream OC-48; processors to be sending transmit data in frame alignment. These signals are driven synchronously with the TXD{3.0}_CLK155P/N signals. These signals are asserted for a single 155MHz clock period when active. These outputs may be optionally operated at CMOS levels when the FRSYNC_CMOS bit is s3et in the G_CR0 register.
TXD{3:0}_VREF (Input)	Transmit Demux {Ports 3:0} Voltage REFerence. These inputs are used to supply the input center voltage around which the single ended LVPECL input buffers should switch. These pins provide the center reference voltage for the TXD{3:0}_FRSYNCH output signals.
T_192C_DETB (Input)	Transmit 192C DETect (Bar). This input signal is driven in a wire or manner from the four external OC-48 processors. The front-end ASIC monitors this signal and uses it to determine if an AIS insertion should be made on the TXL line side output signal. (Note: current implementation does not use this input signal.)
RXL_LOSB (Input)	Receive Line Loss Of Signal (Bar). Input that is received directly from the line side optics module to indicate loss of light.
R_FP <or> *Test (Output)	Receive Port Frame Pulse or Test function. Signal that indicates the position of the framing on the RXL receive line input port. This signal is driven high on the clock cycle following the second A2 byte having been received. The signal remains asserted for twenty-four 622MSz-clock periods. When used externally, a rising edge detection should be used to detect the assertion of this signal. This signal marks the start of unframed data in the R_TDM and R_WCC serial channels.
R_TDM_DAT	Receive TDM Serial DATa or Test function. Serial data output that

Pin Name (I/O Type)	*Pin Description*
<or> *Test (Output)	has been extracted from the receive line side overhead bytes (J0, E1, F1, E2, D1-D12). This output changes on the falling edge of R_TDM_CLK and is latched by external devices on the rising edge of R_TDM_CLK.
R_TDM_CLK <or> *Test (Output)	Receive TDM ClocK or Test function. Output clock used to clock serial data on the R_TDM_DAT pin. R_TDM_DAT pin changes on the falling edge of this clock.
R_WCC_DAT <or> **Test** (Output)	Receive WARP Communication Channel DATa or Test function. Serial data output that has been extracted from the receive line side D4, D5, and D7 overhead bytes as specified in the WCCR register). This output changes on the falling edge of R_WCC_CLK and is latched by external devices on the rising edge of R_WCC_CLK.
R_WCC_CLK <or> **Test** (Output)	Receive WARP Communication Channel ClocK or Test function. Output clock used to clock serial data on the R_WCC_DAT pin. The R_WCC_DAT data output changes on the falling edge of this clock.
T_FP <or> **Test** (Output)	Transmit Port Frame Pulse or Test function. Signal that indicates the position of the framing on the TXL line output port. This signal is driven high on the clock cycle when the 3rd and 4th A2 bytes are on the TXL output data port and remains asserted for twenty-four 622MHz-clock periods. This signal is used to mark the start of unframed data in the T_TDM and T_WCC serial channels.
T_TDM_DAT <or> *Test (Input)	Transmit TDM Serial DATa or Test function. Serial data input used for data to be inserted into the transmit line side overhead bytes (J0, E1, F1, E2, and D1-D12). This input is latched on the rising edge of T-TDM_CLK and is updated by external interface devices on the falling edge of T_TDM_CLK. A pull-up resistor is included on this pin to hold pin state when the input is unused.
T_TDM_CLK (Output)	Transmit TDM ClocK. Output clock used to clock serial data on the T_TDM_DAT pin. The T_TDM_DAT data input is latched on the rising edge of this clock.
T_WCC_DAT (Input)	Transmit WARP Communication Channel DATa. Serial data input used for data to be inserted into the transmit line side D4, D5, and D7 line overhead bytes. This input is latched on the rising edge of T_WCC_CLK and is updated by external interface devices on the falling edge of T_WCC_CLK. A pull up resistor is included on this pin to hold pin state when the input is unused.
T_WCC_CLK (Output)	Transmit WARP Communication Channel ClocK. Output clock used to clock serial data on the T_WCC_DAT pin. The T_WCC_DAT data input is latched on the rising edge of this clock.

Pin Name (I/O Type)	*Pin Description*
CSB (Input)	Chip Select (Bar). Chip select input or the CPU interface. This input must be active to address the front-end ASIC internal registers.
ADDR[10:1] <or> *Test (Input)	CPU interface ADDRess [10:1] input or Test function. Driven by external on-board CPU. Fused to address internal device registers.
DATA[15:0] (bi-directional)	CPU interface DATA bus. Bi-directional data bus used to transfer data to and from the internal on-board CPU. Used to address internal device registers.
RSTB (Input)	ReSeT (Bar) signal. Asynchronous input used to reset the device. Signal is active low input.
RWB (Input)	Read/Write (Bar) Read/Write indication. A high on this signal indicates a read cycle and a low indicates a write cycle.
OENB (Input)	Output Enable (Bar). The output enable for the CPU Data bus. This input must be driven during CPU read cycles to enable the DATA [15:0] data bus.
CPU_TS_B (Input)	CPU Transaction Start (Bar). Indicates the start of a CPU bus cycle.
INTRB (Output)	INTeRrupt (Bar). An interrupt signal used t indicate a pending interrupt from the front-end ASIC device. This is an open collector output and requires a pullup resistor on the PCB.
CPU_CLK (Input)	CPU ClocK input. This input is supplied by the external CPU and is used to synchronize register read/write operations to the CPU bus rate.
CLK_32KHZ (Input)	ClocK 32KHZ input. A 32KHZ input clock used for timing of out-of-frame, loss-of-frame and loss-of-signal.
BIAS {3.0}_Y1 (RB), BIAS {3.0}_YV (VB), (Input) BIAS {3.0}_Z1 (RB), BIAS {3.0}_ZV (VB), (Input) BIAS_K1 (RB), BIAS_KV (VB), (Input) BIAS_J1 (RB), BIAS_JV (VB),	BIAS {3.0} Circuit Y Icc Reference, BIAS {3.0} Circuit Y Voltage Reference, BIAS {3.0} Circuit Z Icc Reference, BIAS {3.0} Circuit Z Voltage Reference, BIAS Circuit K Icc Reference, BIAS Circuit K Voltage Reference, BIAS Circuit J Icc Reference, BIAS Circuit J Voltage Reference, These pins are used to control the generation of the source and sink currents for the LVPECL output buffers. Each bias circuit powers 9 LVPECL outputs. There are ten individual BIAS circuits described in this group. Each of the four demux side ports (as indicated by the 3:0 designation) contains a Y and a Z BIAS circuit. Each bias

Pin Name (I/O Type)	*Pin Description*
(Input)	circuit has a voltage and a current reference input. This BIAS circuits control output pins (on the respective demux side ports) as follows: BIAS{}_Y: TXD{}_CLK155P/N, RXD{}_CLK155P/N, and RXD{}_DATA[15:9] BIAS{}_Z: RXD{}_DATA[8:0] BIAS_K: RXD[1.0]_BPCLKP/N, TXD {3:2}_FRSYNC. BIAS_J: RXD[3.2]_BPCLKP/N, TXD {1:0}_FRSYNC, RXD_REFCK155P/N. See *Section 13.5, "LVPECL Bias Circuits and Terminations"* for recommended external BIAS circuit connections.
TST_CFG[2:0] (Input)	TeST ConFiGuration inputs [2:0]. These inputs are used to enable the different possible test modes of the device. These inputs include pull down resistors such that normal device operating mode is selected when these inputs are left unconnected. See *Section 11, "TEST Modes and Features"* for information on the function and usage of this pins.
NAND_CHN (Output)	NAND ChaiN. This pin is the output of the internal NAND Chain used for output pin DC level testing. This output pins is normally tristated and only becomes active when the Input Levels Test Mode is selected via the TST_CFG[2:0] test configuration pins. See *Section 11, "TEST Modes and Features"* for information on the function and usage of this pins.
VREFH (PWR)	High reference voltage and bias current supply for all LVDS type output drivers.
VREFL (PWR)	Low reference voltage and bias current supply for all LVDS type output drivers.
VDD3 (PWR)	3.3V IO VDD Supply. Used for all TTL type and all LVPECL type IO buffers.
VDD2 (PWR)	2.5V Core VDD Supply. Used for internal device core logic and for the digital logic portions of the LVDS IO buffers.
VSS (PWR)	Ground connection for IO buffers and core logic.